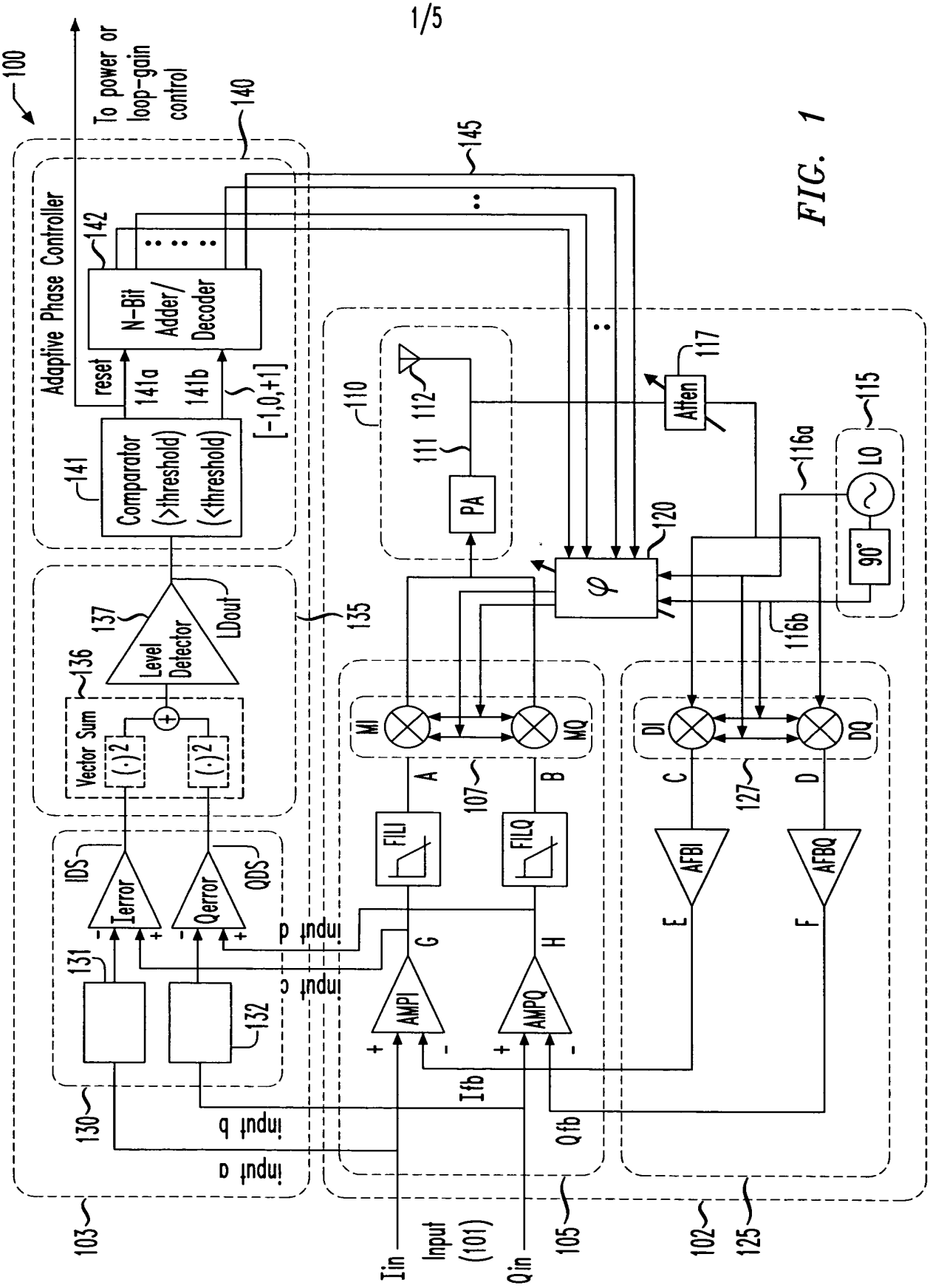
100
To power or loop-gain control
140
145
Adaptive Phase Controller
142
N-Bit Adder/ Decoder
reset
141a
141b
[-1,0,+1]
141
Comparator (>threshold) (<threshold)
110
111
112
PA
117
Atten
115
LO
116a
90°
120
φ
116b
135
137
Level Detector
LDout
136
Vector Sum
(·)2
(·)2
MI
MQ
DI
DQ
107
127
A
B
C
D
FILI
FILQ
AFBI
AFBQ
E
F
IDS
Terror
Qerror
QDS
131
132
G
H
AMPI
AMPQ
Ifb
Qfb
input d
input c
input b
input a
130
103
105
102
125
Iin
Input (101)
Qin

FIG. 1

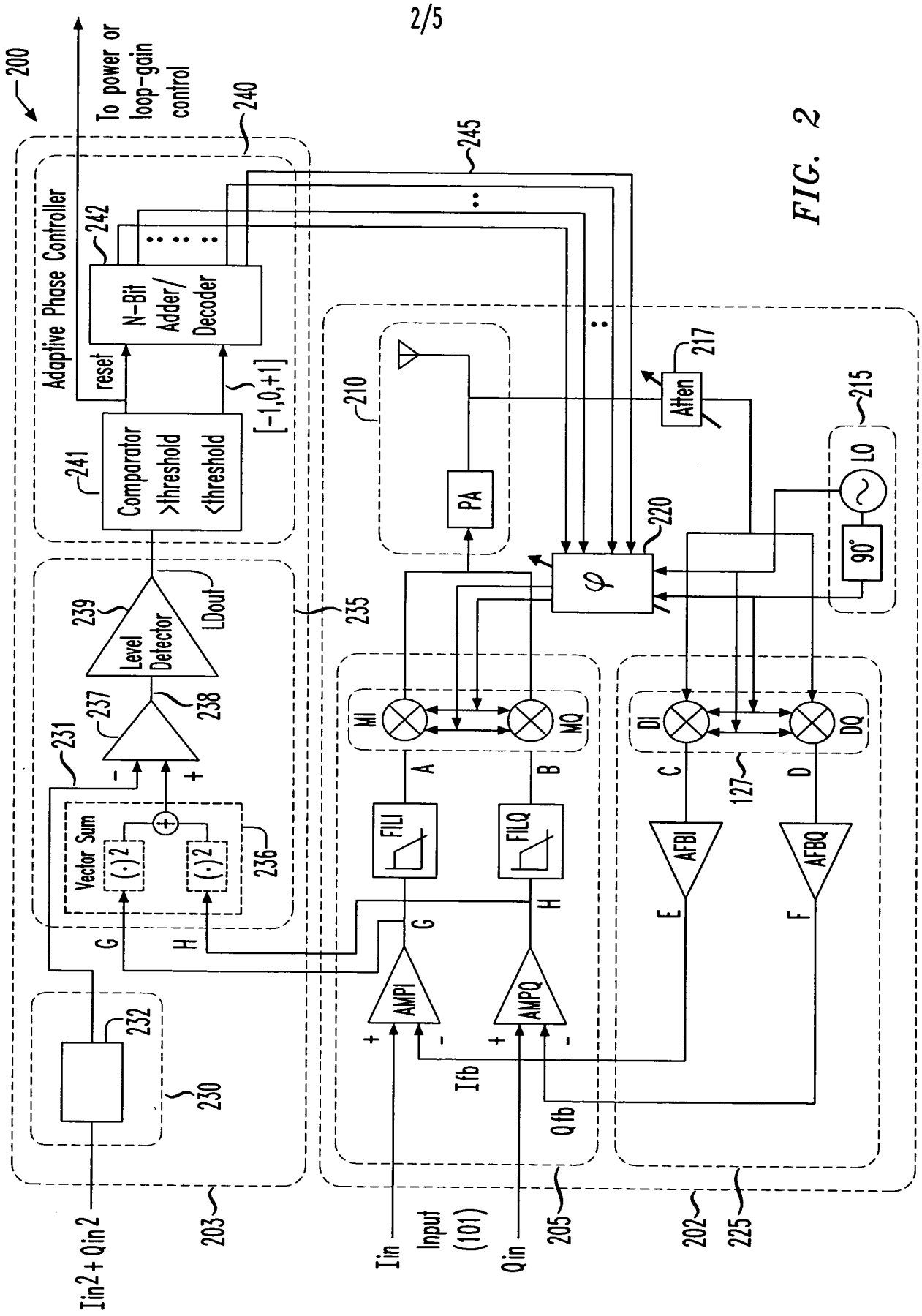
200
To power or loop-gain control
240
Adaptive Phase Controller
242
N-Bit Adder/ Decoder
reset
[-1,0,+1]
241
Comparator >threshold <threshold
245
210
PA
217
Atten
215
LO
90°
220
φ
235
239
Level Detector
LDout
237
238
231
Vector Sum
(·)2
236
MI
MQ
DI
DQ
A
B
C
D
127
FILI
FILQ
AFBI
AFBQ
E
F
G
H
AMPI
AMPQ
Itb
Qtb
232
230
203
205
202
225
Iin2 + Qin2
Iin
Input (101)
Qin

FIG. 2

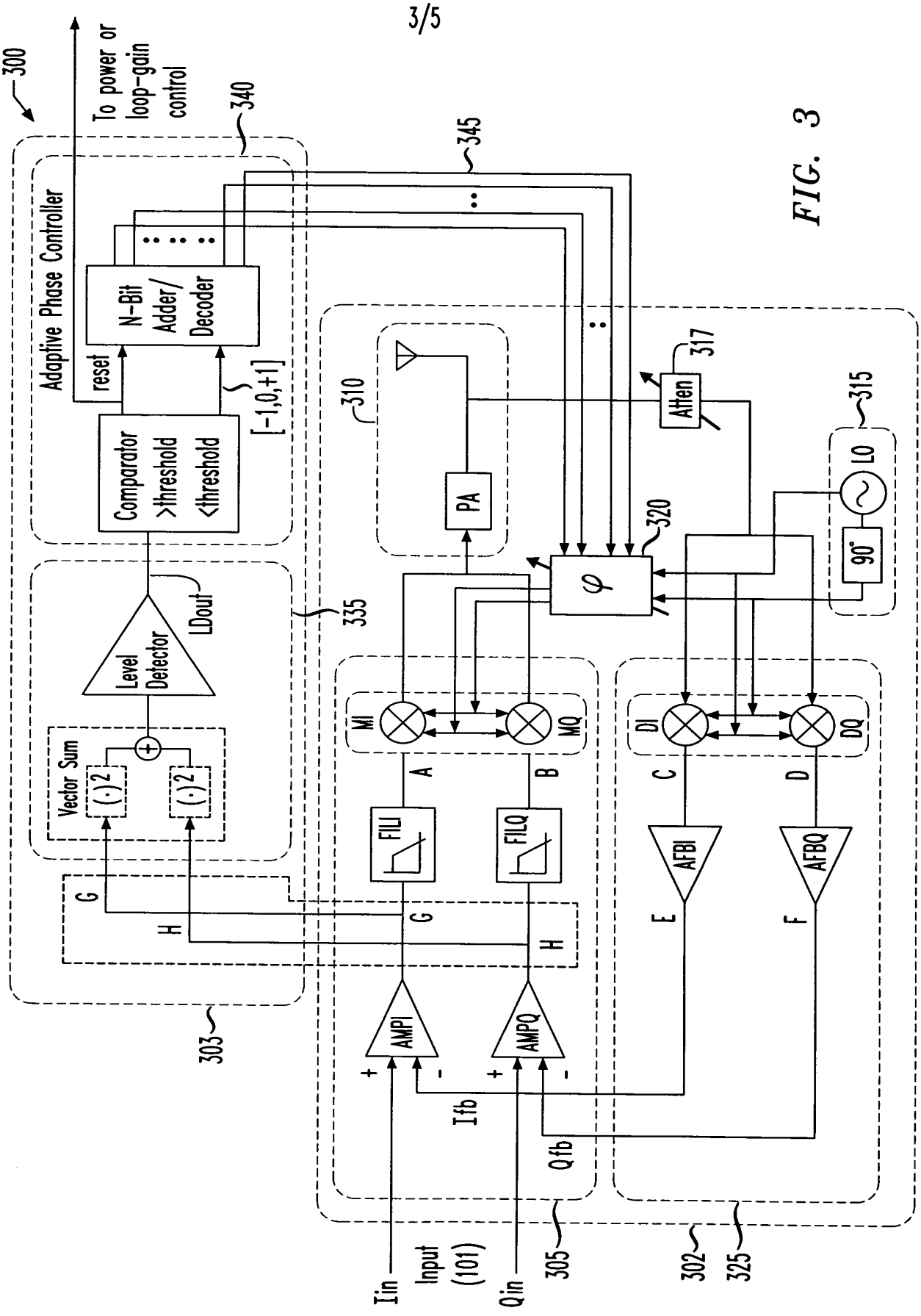
300
To power or loop-gain control
340
345
Adaptive Phase Controller
N-Bit Adder/ Decoder
reset
[-1,0,+1]
Comparator >threshold <threshold
310
PA
317
Atten
315
LO
90°
320
φ
335
Level Detector
LDout
Vector Sum
(·)2
(·)2
MI
MQ
DI
DQ
A
B
C
D
FILI
FILQ
AFBI
AFBQ
E
F
G
H
G
H
AMPI
AMPQ
+
-
+
-
Ifb
Qfb
303
305
302
325
Iin
Input (101)
Qin

FIG. 3

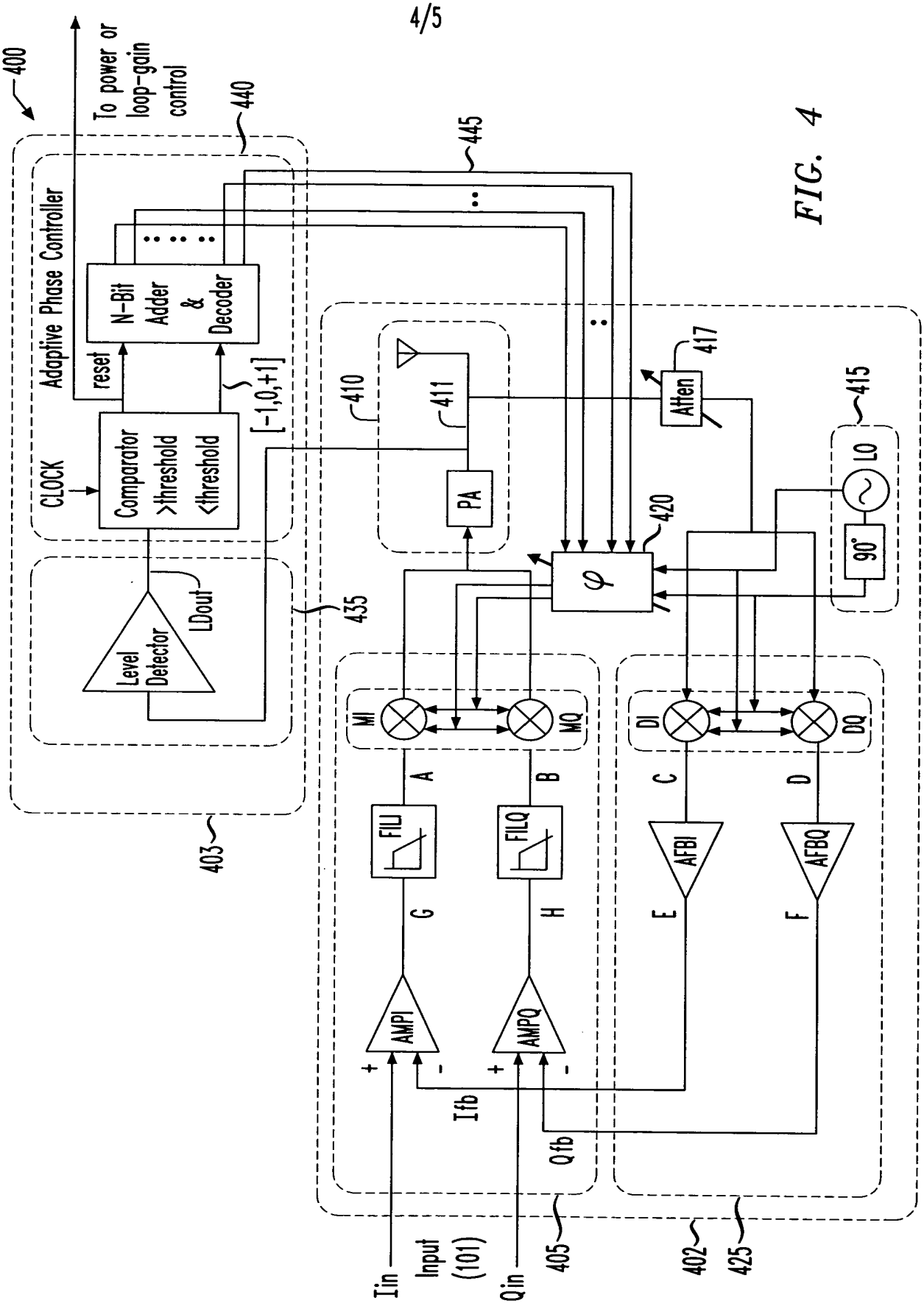
400
To power or loop-gain control
440
445
Adaptive Phase Controller
N-Bit Adder & Decoder
reset
[-1,0,+1]
CLOCK
Comparator >threshold <threshold
Level Detector
LDout
435
403
410
411
PA
417
Atten
415
LO
90°
420
φ
MI
MQ
DI
DQ
A
B
C
D
FILI
FILQ
AFBI
AFBQ
G
H
E
F
AMPI
AMPQ
+
-
Ifb
Qfb
Iin
Input (101)
Qin
405
402
425

FIG. 4

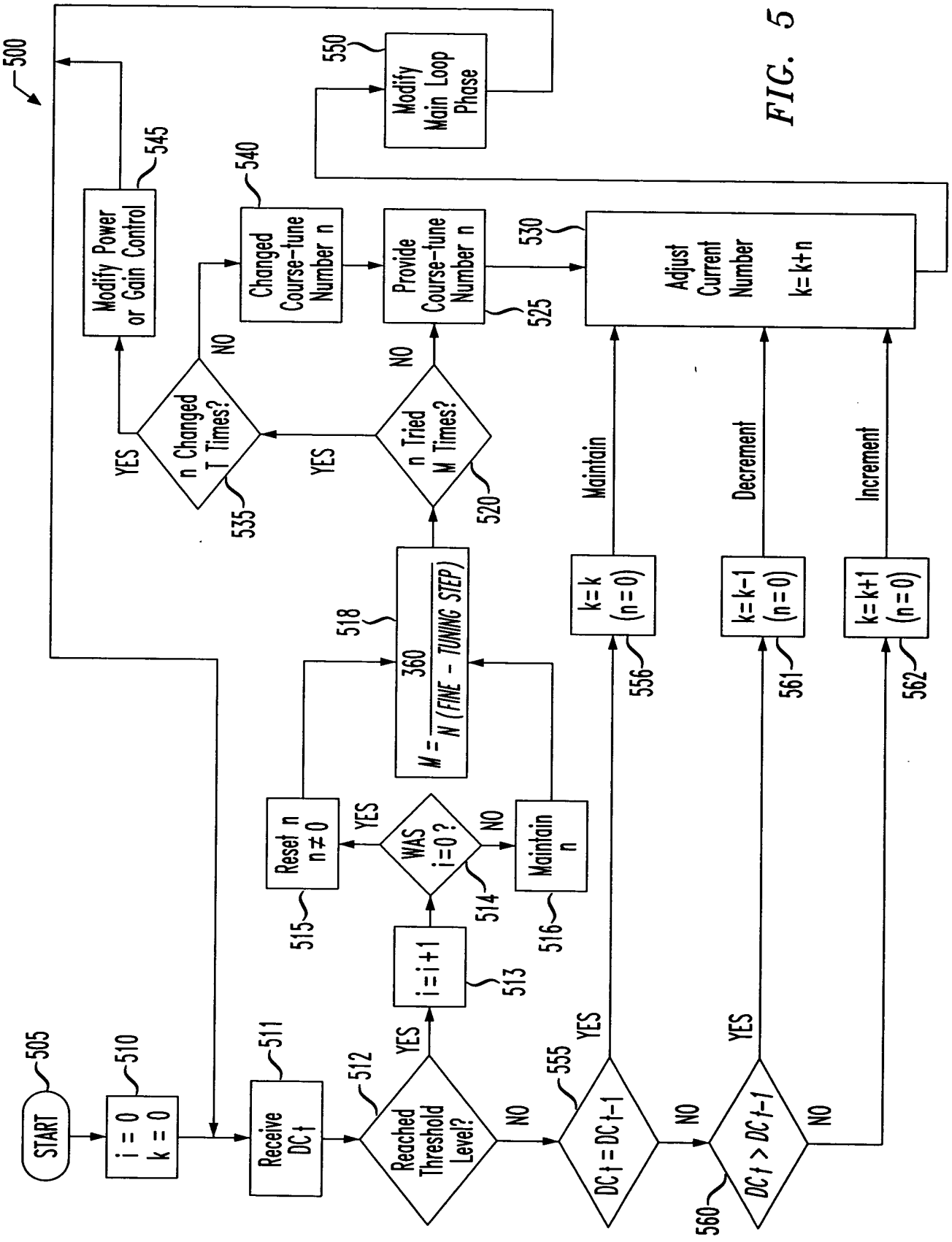
500
505
START
510
i = 0
k = 0
511
Receive DC t
512
Reached Threshold Level?
YES
NO
513
i = i + 1
514
WAS i=0 ?
YES
NO
515
Reset n
n ≠ 0
516
Maintain n
518
M = 360 / N (FINE - TUNING STEP)
520
n Tried M Times?
YES
NO
525
Provide Course-tune Number n
530
Adjust Current Number
k= k+n
535
n Changed T Times?
YES
NO
540
Changed Course-tune Number n
545
Modify Power or Gain Control
550
Modify Main Loop Phase
555
DC t = DC t-1
YES
NO
556
k= k
(n = 0)
Maintain
560
DC t > DC t-1
YES
NO
561
k= k-1
(n = 0)
Decrement
562
k= k+1
(n = 0)
Increment

FIG. 5